Low phase noise and low jitter 0.1-10GHz VCO

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Outline

- Introduction & Motivations
- Q-factor definition and calculation
- Review of classical VCO topologies
- Discussion on phase noise and LC tank design
    - Choice of L and C_V to optimize phase noise power performances
- Presentation of low voltage VCO structure suitable for high swings
- 2.4GHz 65nm CMOS BLE VCO measurement results
- Alternative synthesizer architecture based on FBAR
    - Performance comparison with LC/XO PLL

PLL performance is limited by XTAL and VCO phase noise

Close-in noise limited by:

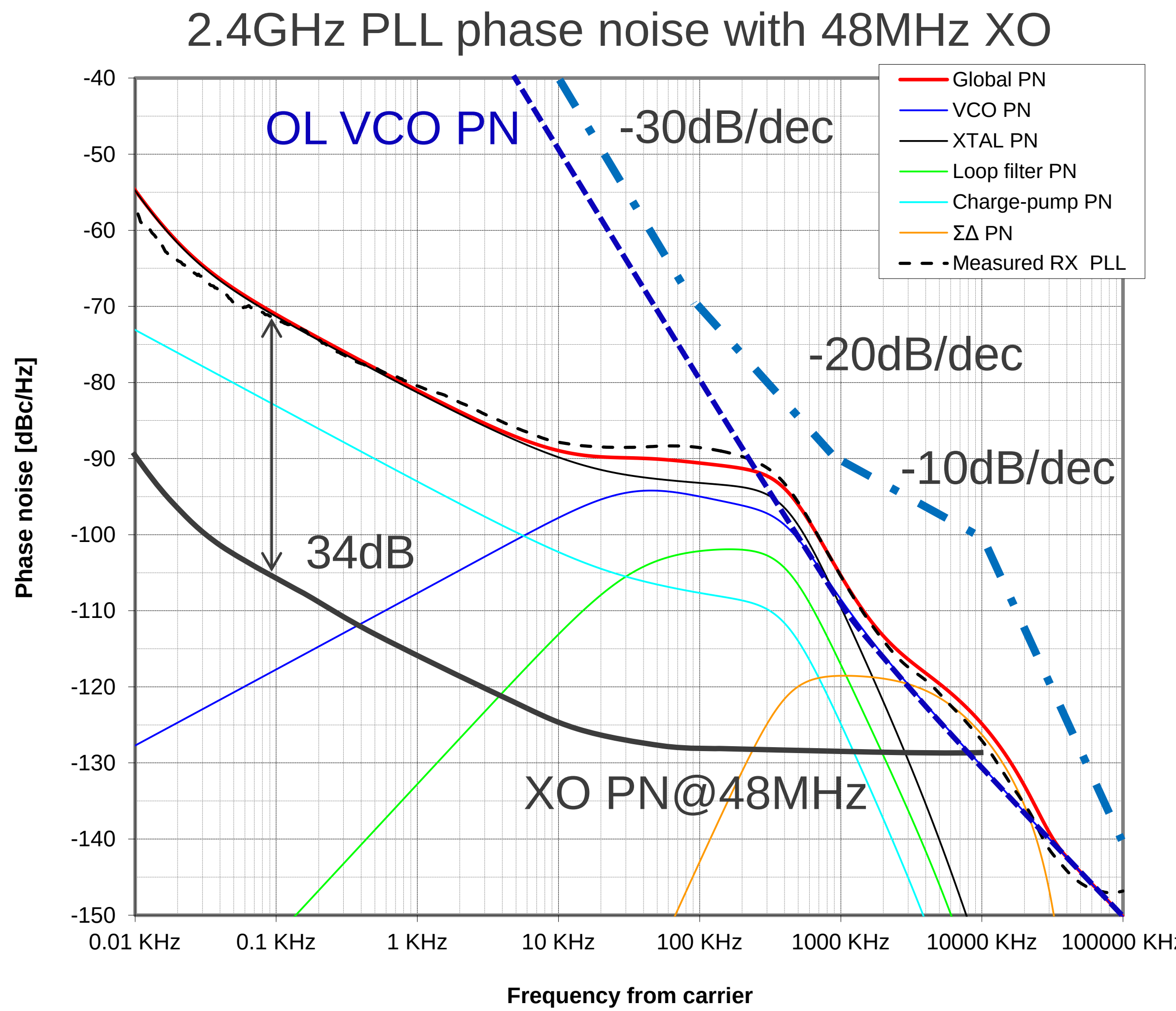
- XO phase noise
- Increased by 20 log(N)

Far-from-carrier noise by:

- VCO phase noise

PLL Loop BW

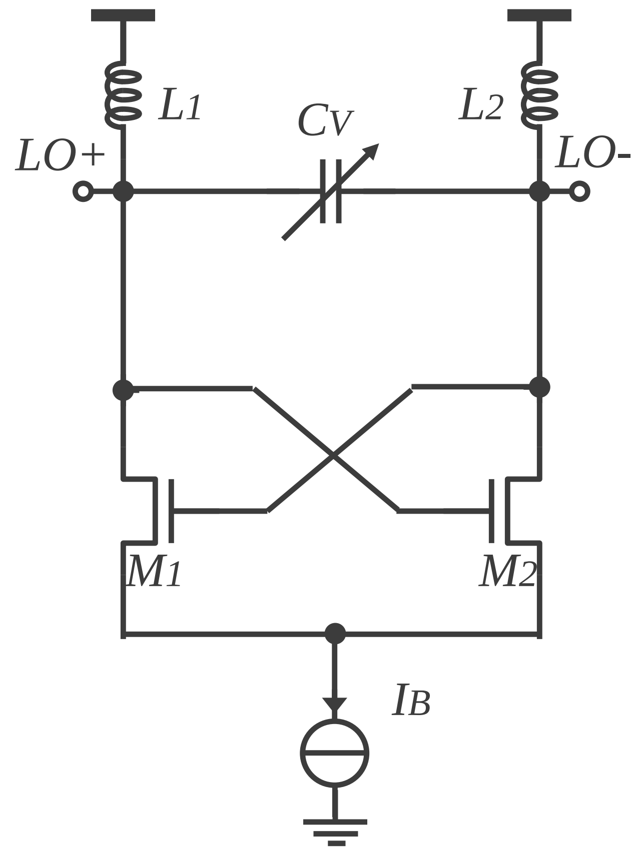
- Chosen when those noise sources are equal



Simple VCO structure

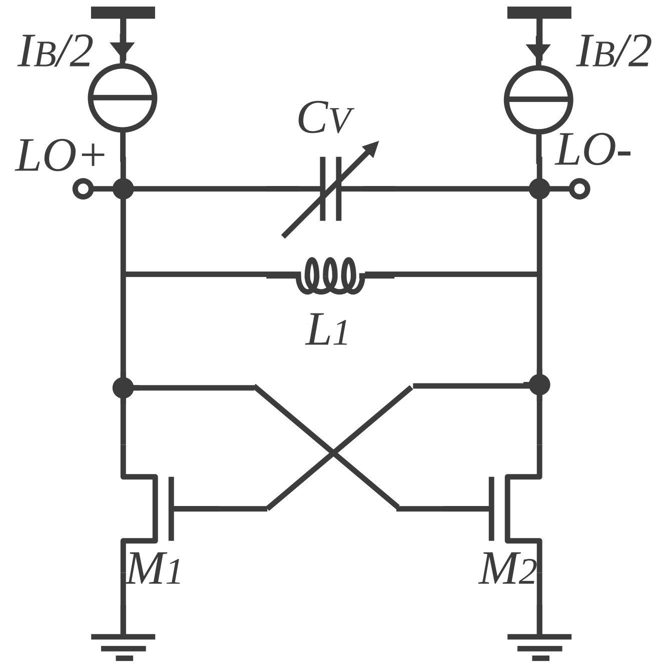
- Cross-coupled pair provides negative conductance
  - $-g_m/2$ with $g_m = I_B/(2 \cdot n \cdot U_T)$ in sub-T
- Should balance tank loss ($g_P = 1/R_P$)
  - Calc R_P with series/parallel transformation
- Large swing feasible ($\sim 2 \cdot V_{CC}$)
- Barkhausen criterion

$$\omega_o = \sqrt{\frac{1}{L \cdot C}} \qquad g_m \cdot R_P = -1$$



Another simple VCO structure

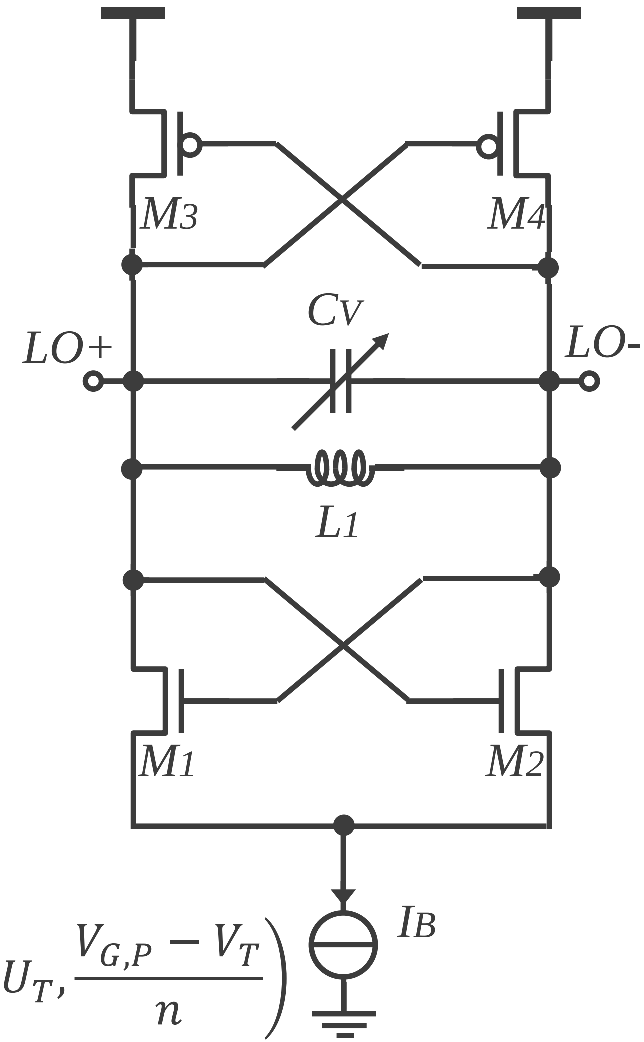
- Current can be fed on both drains if only a 2 terminals single coil is available
  - Drain junction cap loading tank
  - Limited swing $(V_{CC}-V_{DSAT})/2$
- Feed inductor midpoint instead
  - Same $V_{OSC}(I_B)$ as calculated for XO
  - Large swing feasible
- What happens if constant V_{CC} bias?
  - Current keeps increasing until $M_{1,2}$ leave saturation
  - Strong non-linearity reduces gain
  - Leads to increased phase noise



Complementary VCO structure (most popular)

- Equivalent to two cross-coupled inverters
- Could potentially halve bias current
  - g_m of PMOS usually lower as same W/L
- Ampl. control with one biasing current source
  - Without I_B, desaturation and PN degradation
- Poor PSRR: LDO can be used to provide clean V_{CC}
- Sensitive to PVT variations, limited V_{OSC} at low V_{CC}
- Watch-out for proper start-up in SS, V_{MIN}, T_{LOW}
- Operation in sub/near threshold permit higher swings owing to a reduced V_{DSAT}
- With $V_{G,P}$ the peak gate voltage

$$V_{DSAT} = max\left(5 \cdot U_T, \frac{V_{G,P} - V_T}{n}\right)$$



How to optimize the phase noise power product of a VCO

- Noise

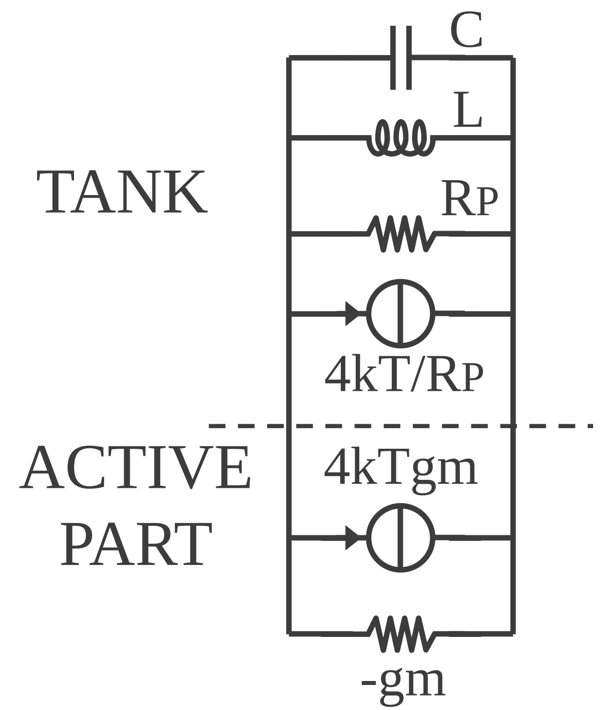
$$\phi_n = \frac{(1+\gamma)\cdot kT}{Q} \cdot \sqrt{\frac{L}{C}} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \cdot \frac{1}{V_{OSC}^2}$$

- Power

$$I_{OSC} \cdot V_{DD} \rightarrow \left. \frac{V_{OSC} \cdot V_{DD}}{\sqrt{\frac{L}{C}} \cdot Q} \right|_{V_{OSC} >> 0}$$

- Noise x Power

$$\phi_n \cdot P_{OSC} \propto \frac{(1+\gamma)}{Q^2} \cdot \frac{V_{DD}}{V_{OSC}}$$



To get lower PN

1. Max Q
2. Max V_{OSC}
3. Min γ
4. Increase C

$$\omega_o = \sqrt{\frac{1}{L \cdot C}}$$

$$g_m \cdot R_P = -1$$

How to design the VCO tank? (obviously an iterative process!)

- Selection of coil type
  - External coil — Q up to 100, up to 2-3GHz, reproducibility of PCB
  - Bondwire — Very good Q but reproducibility issues (L=1nH/mm)
  - PCB trace, microstrip line — Suitable for SHF, IO modelling + ESD issues
  - Integrated — Attractive above 1GHz, Q~10-20@ 2.4GHz
- Determine the fixed VCO load (C_F) — mixers & PA, buffers, PLL dividers, VCO, routing
- Varactor C_V need to cover — desired BW & all manufacturing tolerances
- Using $k = \dfrac{C_F + C_{V,MAX}}{C_F + C_{V,MIN}}$ and $k' = \dfrac{C_{V,MAX}}{C_{V,MIN}}$ $\qquad \dfrac{\Delta f}{f} = \dfrac{1}{2} \cdot \left(\dfrac{\Delta C}{C} + \dfrac{\Delta L}{L} + BW \right)$
- The tuning range and the min varactor size can be expressed as

$$TR = \pm \frac{f_{MAX} - f_{MIN}}{f_{MAX} + f_{MIN}} = \pm \frac{\sqrt{k} - 1}{\sqrt{k} + 1} \qquad C_{V,MIN} = \left(\frac{k-1}{k' - k} \right) \cdot C_F$$

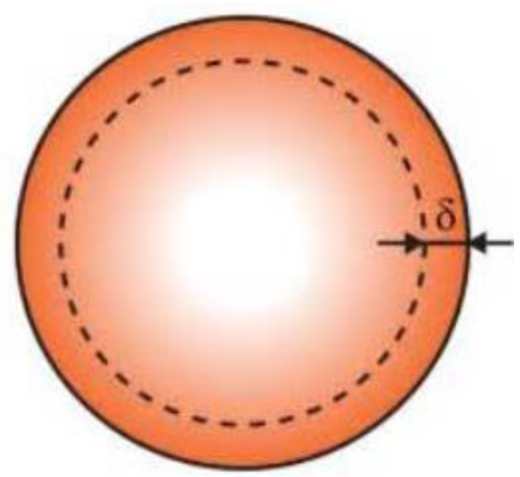
- The max possible inductor value can be determined, phase noise perfs estimated

Coil Q-factor limitation due to skin depth effect

- Skin depth simplified calculation

$$\delta = \sqrt{\frac{2\rho}{(2\pi f)(\mu_0 \mu_r)}} \approx 503 \sqrt{\frac{\rho}{\mu_r f}}$$

  - For copper, $\mu_r = 1$, $\rho = 1.68\text{E-}8\ \Omega\cdot\text{m}$
  - $\delta = 1.33\ \mu\text{m}$ @ 2.4 GHz
  - $\delta = 0.27\ \mu\text{m}$ @ 60 GHz



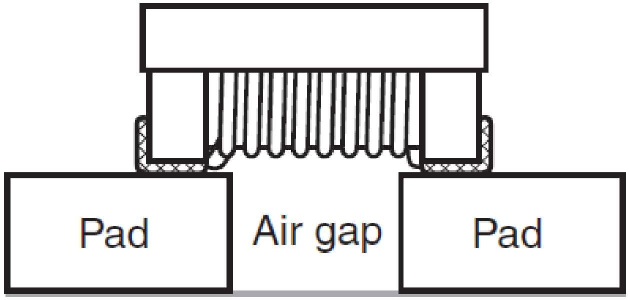
- It can't be neglected
  - Use EM solver to study impact more carefully (e.g. Momentum)

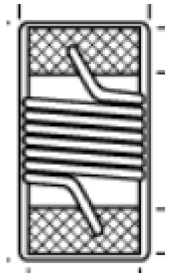
Equivalent model for discrete coils

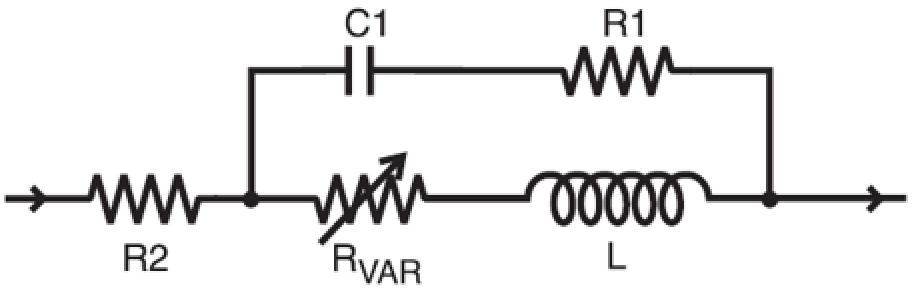
- R_2 is DC resistance
- R_{VAR} accounts for skin effect

$$R_{VAR} = \mathrm{k} \cdot \sqrt{f} \qquad \text{k in } [\Omega \cdot s^{0.5}]$$

- C_1 defines Self Resonance Frequency
- R_1 & R_{VAR} define Q @ SRF
- Model PCB, bondwire, bumps, PADS, routing wires properly (L=1nH/mm)
- Use S/P transformations to get Q_L

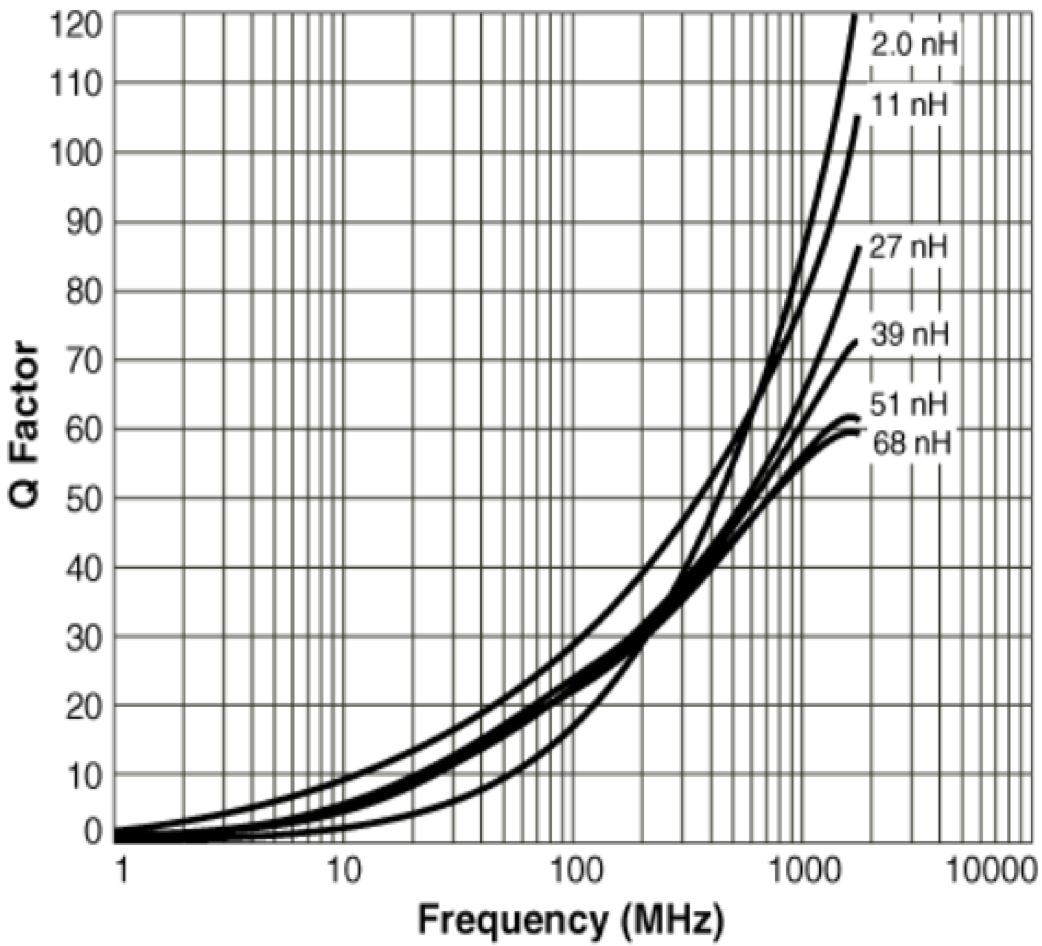






Part number	R1 (Ω)	R2 (Ω)	C (pF)	L (nH)	k	Upper limit (MHz)
0402HP-1N0	6	0.038	0.030	1.00	2.70E-06	20000
0402HP-2N0	5	0.038	0.050	2.00	5.22E-06	20000
0402HP-2N2	4	0.038	0.040	2.20	5.70E-06	20000
0402HP-2N4	13	0.042	0.044	2.40	6.20E-06	20000
0402HP-2N7	11	0.056	0.044	2.70	6.46E-06	20000
0402HP-3N3	15	0.045	0.032	3.30	7.80E-06	20000
0402HP-3N6	10	0.045	0.022	3.60	8.10E-06	20000
0402HP-3N9	12	0.045	0.042	3.90	9.70E-06	14000
0402HP-4N3	10	0.040	0.048	4.30	1.12E-05	12000
0402HP-4N7	13	0.060	0.052	4.70	1.29E-05	12000

Typical discrete 402 coil Q-factor and Self Resonance Frequency



Inductance[2] (nH)	Percent tol[3]	900 MHz		1.7 GHz		SRF typ[5] (GHz)
		L typ	Q typ[4]	L typ	Q typ[4]	
1.0	5	0.97	46	0.99	72	16.0
2.0	5	1.96	58	1.98	85	15.2
2.2	5	2.17	60	2.17	86	15.1
2.4	5,3,2	2.37	60	2.38	83	14.0
2.7	5,3,2	2.66	62	2.68	85	13.0
3.3	5,3,2	3.26	66	3.28	95	12.8
3.6	5,3,2	3.56	65	3.58	94	11.7
3.9	5,3,2	3.87	64	3.91	98	9.50
4.3	5,3,2	4.26	63	4.33	90	7.15
4.7	5,3,2	4.67	58	4.74	83	6.85
5.1	5,3,2	5.07	54	5.16	76	6.80

Integrated coils

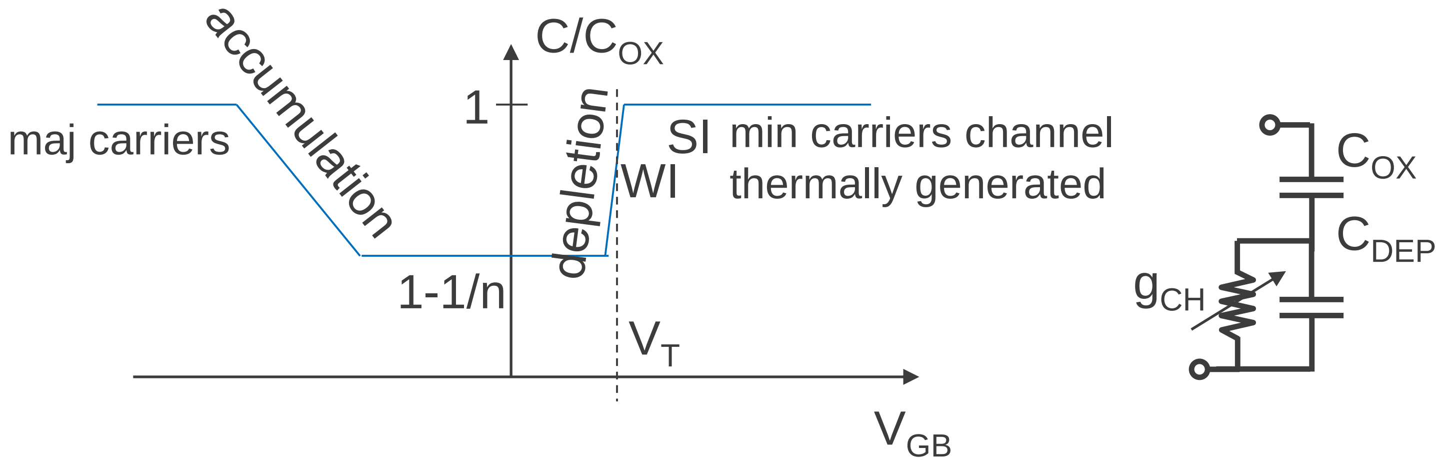
- Use Al RDL (aluminum redistribution layer) + ultra-thick metal process option
- Use RF-PDK coil generator to get expected peformances
  - Usually limited to single layer coil
- Designing your own coil is feasible but requires expertise and is time-consuming
  - Use EM-solver such as e.g. Momentum
  - Difficult to guarantee error free design (LVS is tricky)
  - Multi-layer coils and transformers can be engineered
- Typical performance of a compact integrated coil at 2.4GHz
  - $L=7.9nH$, $R=8\Omega$, $Q=13$, $SRF=7.5GHz$, $C_{SRF}=65fF$, $C_{TOT}=637fF$
- A wider area could lead to better performances

Varactor design

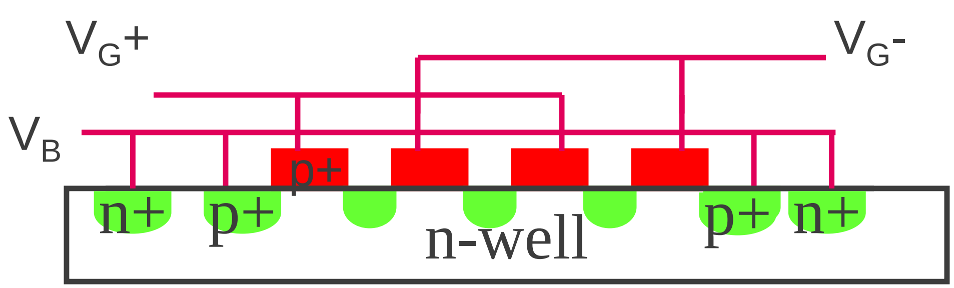
- There are different types of analog varactors
  - Junction diodes, Inversion & accumulation MOS capacitance
- Digitally-controlled varactors can be made with
  - MOM cap and switches
  - Inversion capacitance
- Combined analog and digitally controlled varactor for fine and coarse tuning
- DCO using 2nd order $\Delta\Sigma$ modulator on 3-unit caps for fine frequency interpolation
- Varactor tuning ratio and Q-factor is a compromise

Analog varactor using MOS capacitor (I)

- NMOS C(V) curve (neglecting overlap capacitance)



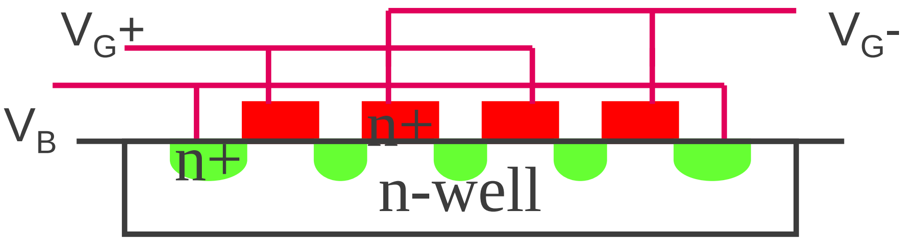
- Inversion or depletion capacitance has very abrupt C(V) change leading to high gain
- Place substrate tap regularly to provide maj carriers as well to prevent Q degradation



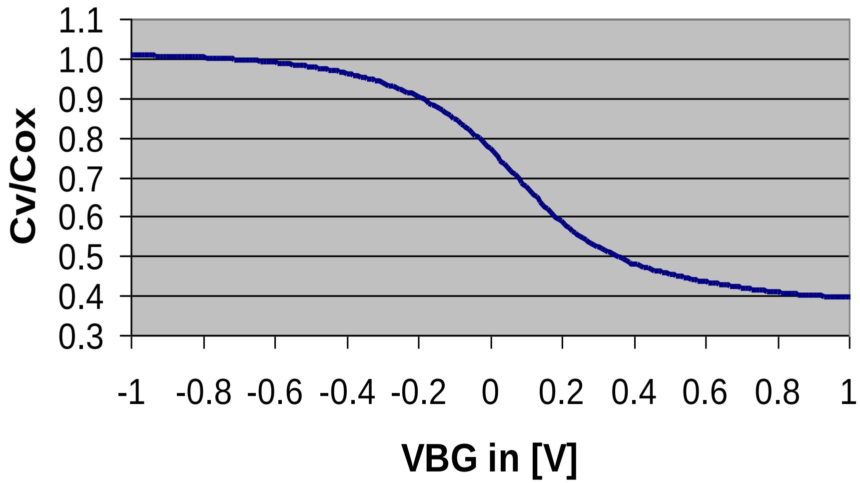
- Q scales as $1/L^2$, watch out for R_G (W)
- Overlap capacitance limit CM/Cm
- Alternate + & - fingers (virtual gnd)
- No contact required in active zone

Analog varactor using MOS capacitor (II)

- Accumulation varactor has lower and more linear dC/dV curve than inversion
- dC/dV curve is max near 0V bias provided G and S/D doping is reverted



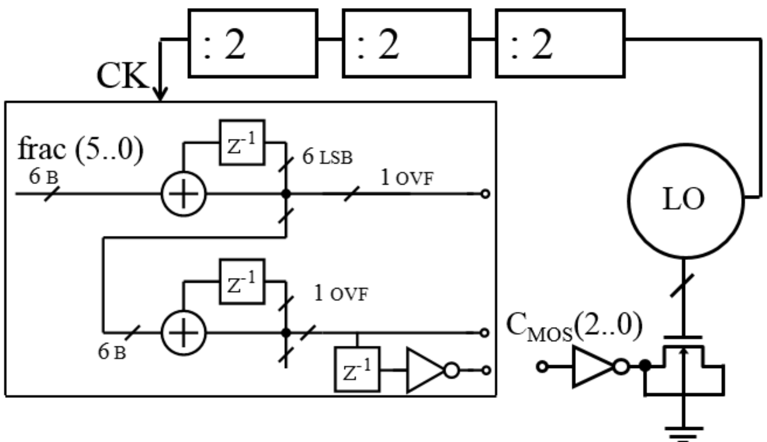
Cv_M / Cv_m = 2.6 (l= 0.46 μm in 0.18 μm CMOS)

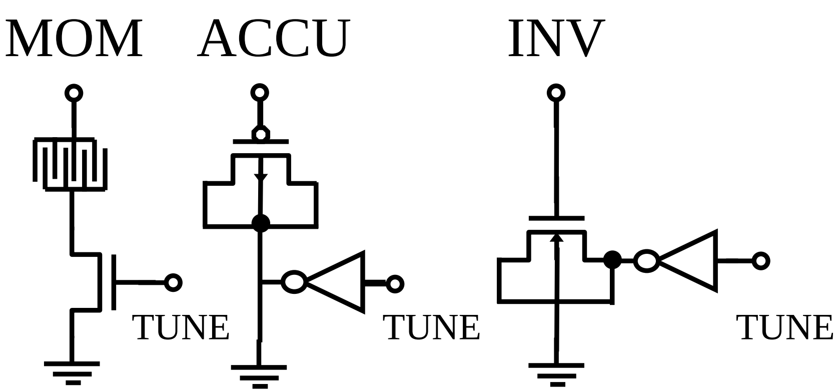


- Equivalent to NMOS in NW or PMOS in PW using triple well
  - Inverse doping shifts curve by V_{BG}
- Q scales as $1/L^2$, watch out for R_G (W)
- Overlap capacitance limit CM/Cm
- Alternate + & - fingers (virtual gnd)
- No contact required in active zone

Digitally controlled varactor

- Finger type fringe MOM capacitor with MOS switch (no V_{CC},V_{CM} dependency on C)
  - Size switch properly to get desired Q ($1/Ron=\beta\cdot(V_{CC}-V_T)$)
  - Parasitic cap (MOS + fringe cap) determines on/off ratio
- Accumulation (switch shorted SDB terminals) or inversion (switch SD) MOSCAP
  - Beware of the common mode potential to operate in low gain zone
- Frequency interpolation can be obtained with ΔΣ modulator for fine tuning

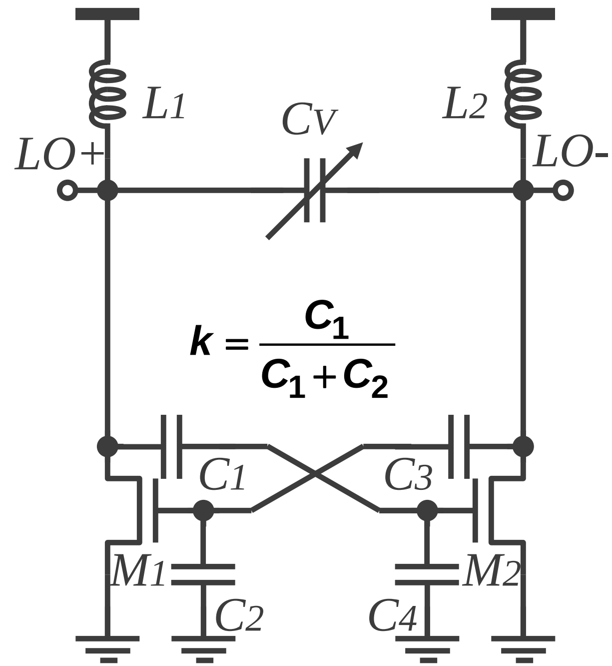




How to get large swings: VCO core structure using cap attenuation

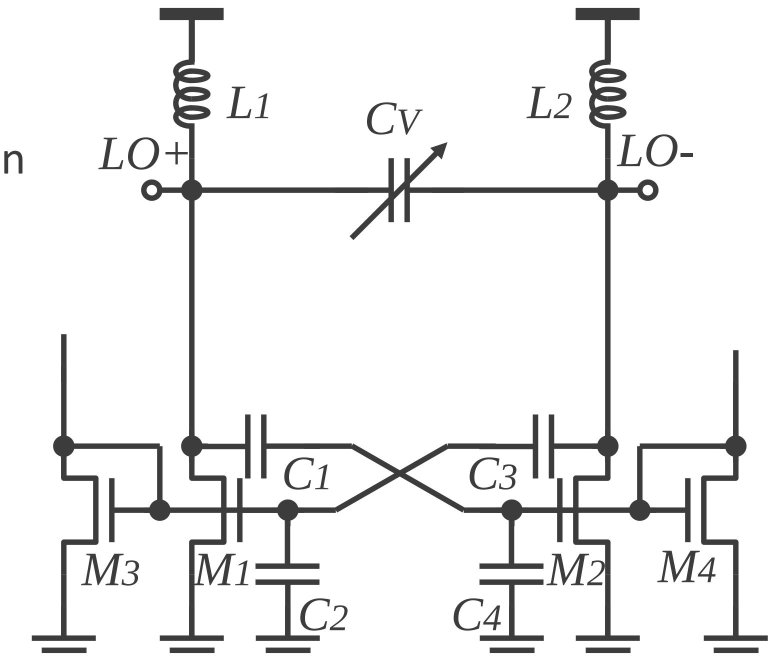
Use capacitive attenuation, k, to

- Linearize MOS and control its biasing
  - Negative gm, V_{OSC} are scaled by 1/k
  - Permit WI operation
- Decouple drain and gate voltages at DC
  - High V_{OSC} / V_{CC} ratio
    - $V_{OSC,MAX} = V_{CC} - V_{DSAT}$
  - No PVT influence on V_{OSC}
- Suitable for very low V_{CC} operation
  - 0.5V VCO with 0.7V diff 0-to-peak feasible



Biasing of the VCO core structure using cap attenuation (I)

- Gate biasing with diode-connected MOS
- I_{VCO} set by mirror ratio (use a fraction for $M_{3,4}$)
- g_m loss scaled by square of attenuation factor
- Resistors can be used to make diode connection
  - Cap at the drain nodes is at CM voltage



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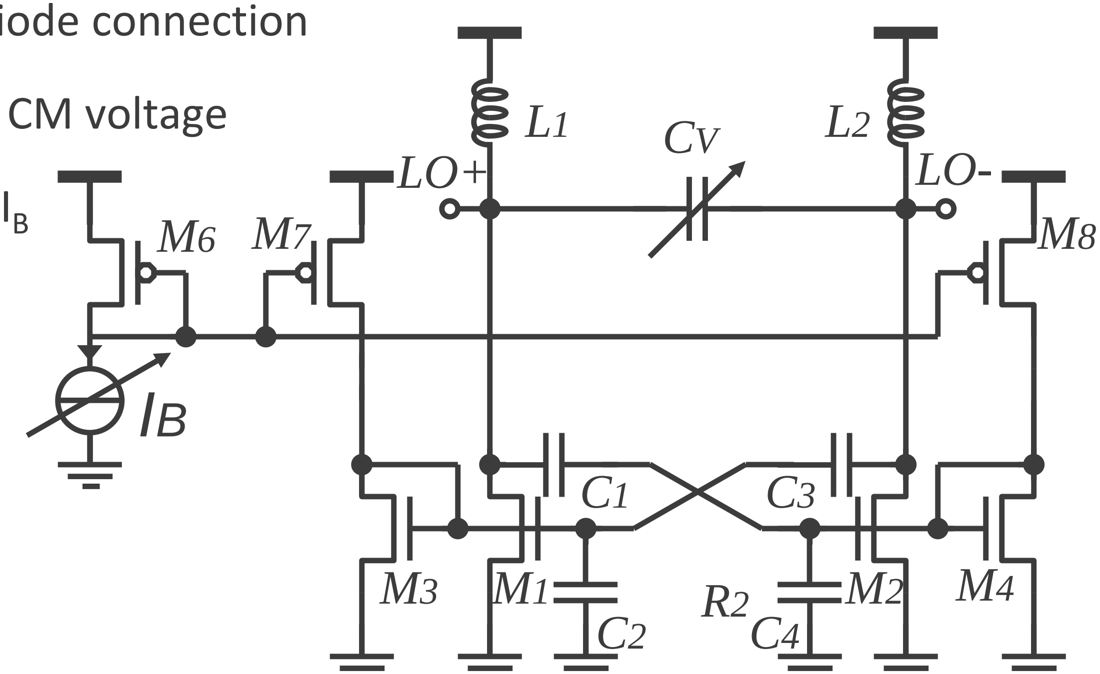
Biasing of the VCO core structure using cap attenuation (II)

- Gate biasing with diode-connected MOS
- I_{VCO} set by mirror ratio (use a fraction for $M_{3,4}$)
- g_m loss scaled by square of attenuation factor
- Resistors can be used to make diode connection
  - Cap at the drain nodes is at CM voltage
- Add $M_{6,7,8}$ mirrors to control via I_B
- Similar $I(V_{OSC})$ behaviour as that derived for XO

$$I_{D_{1\omega}}(A)\frac{I_{B0}\left(\frac{A}{n\cdot U_T}\right)}{2\cdot I_{B1}\left(\frac{A}{n\cdot U_T}\right)}=\overline{I_D}(A)$$



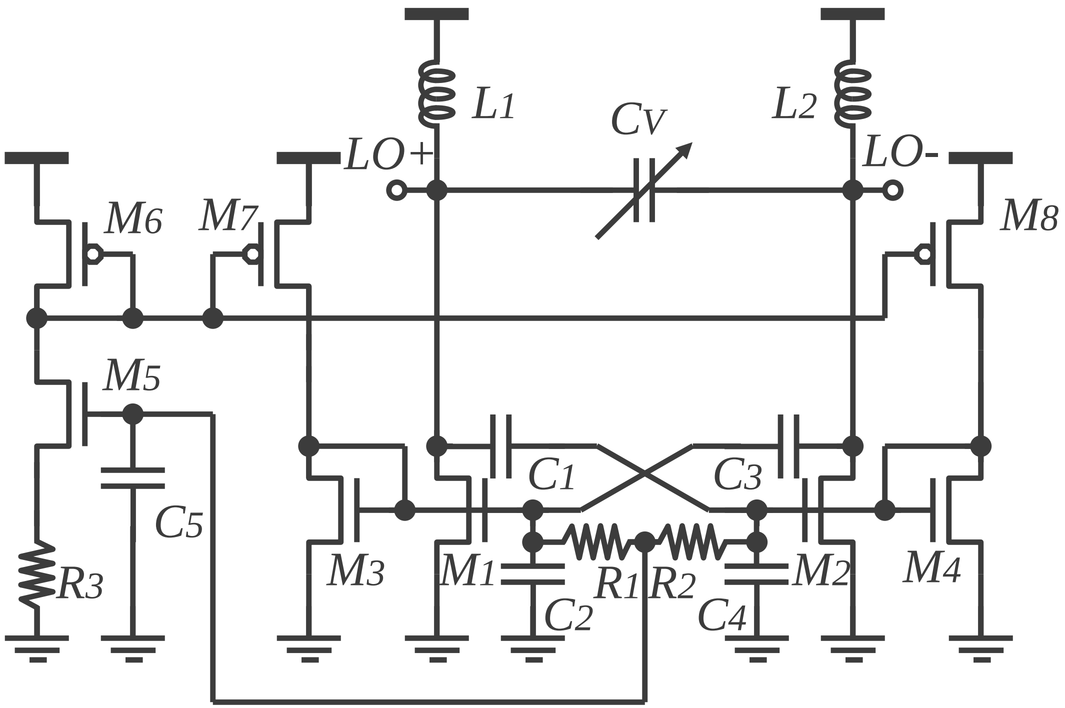
Complete VCO structure including AGC loop

Amplitude regulation formed by

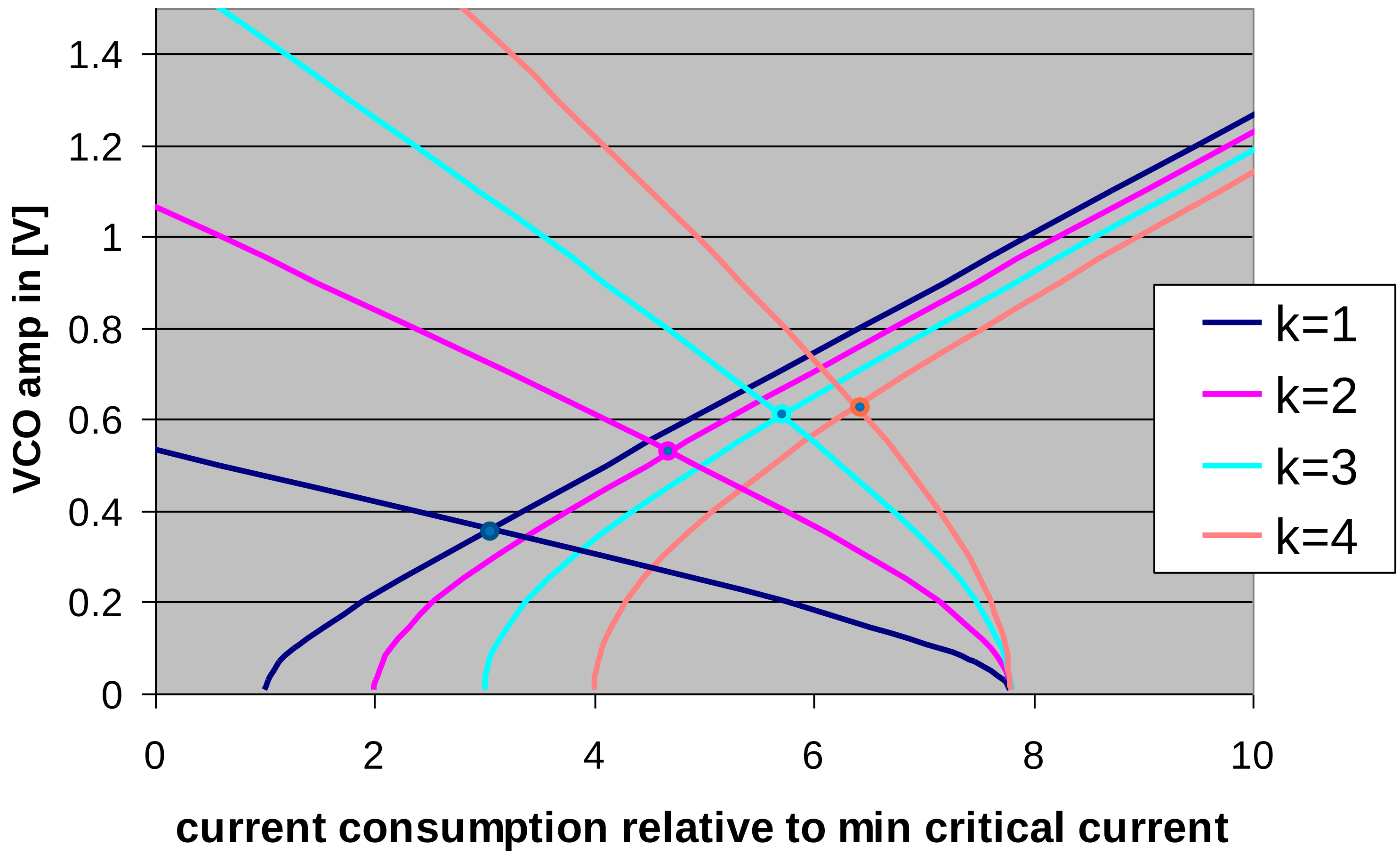
- R1,R2,C5 (BW)
- M5,R3 (PTAT I_{REF})

Benefits

- constant amplitude
  - insensitive to dQ, dC
- Suppression of amplitude noise
  - Min AM to PM conversion
  - 1/f noise of $M_{1,2}$
- Min power consumption
- Great design freedom

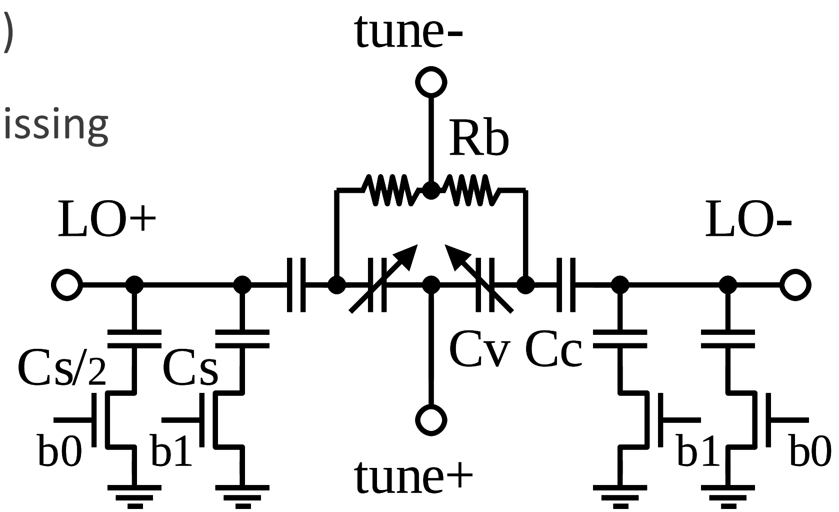


V_{OSC} vs I for VCO & REG and different k values



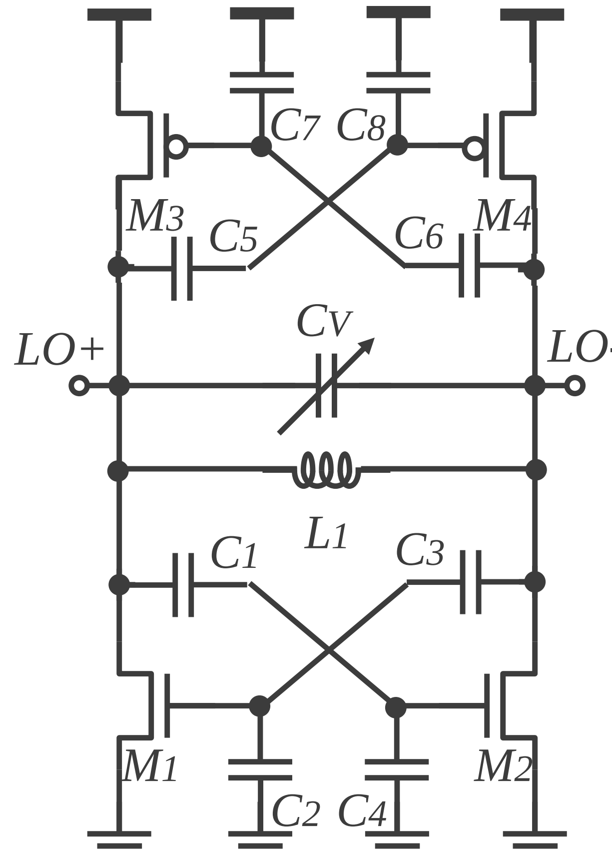
Details of the varactors implementation

- AC-coupled accumulation varactors can be used (dC/dV max near 0V!)
  - Yields differential tuning (good at low V_{CC})
  - Much better PSRR
- Size properly the resistors (Q-degradation)
- Study common-mode behaviour to add missing elements & watch-out for added pole!
- Coarse tuning obtained with SC-C_{MOM}
  - Ensure sufficient overlap with $C_{V,ANA}$
  - Obviously more than 2 bits feasible



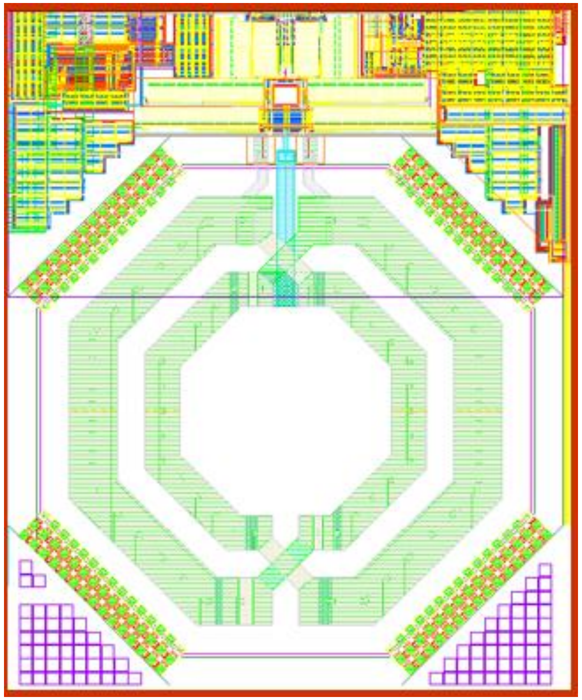
Complementary AC-coupled VCO topology

- Relaxed phase noise or V_{OSC} requirements ?
  - Complementary structure may halve P_{DISS}
  - V_{OSC} up to $(V_{CC} – V_{DSAT})/2$
- Implement biasing, AGC and CM ctrl loops
- Truly low voltage structure
  - V_{CC} = 1V over PVT in production



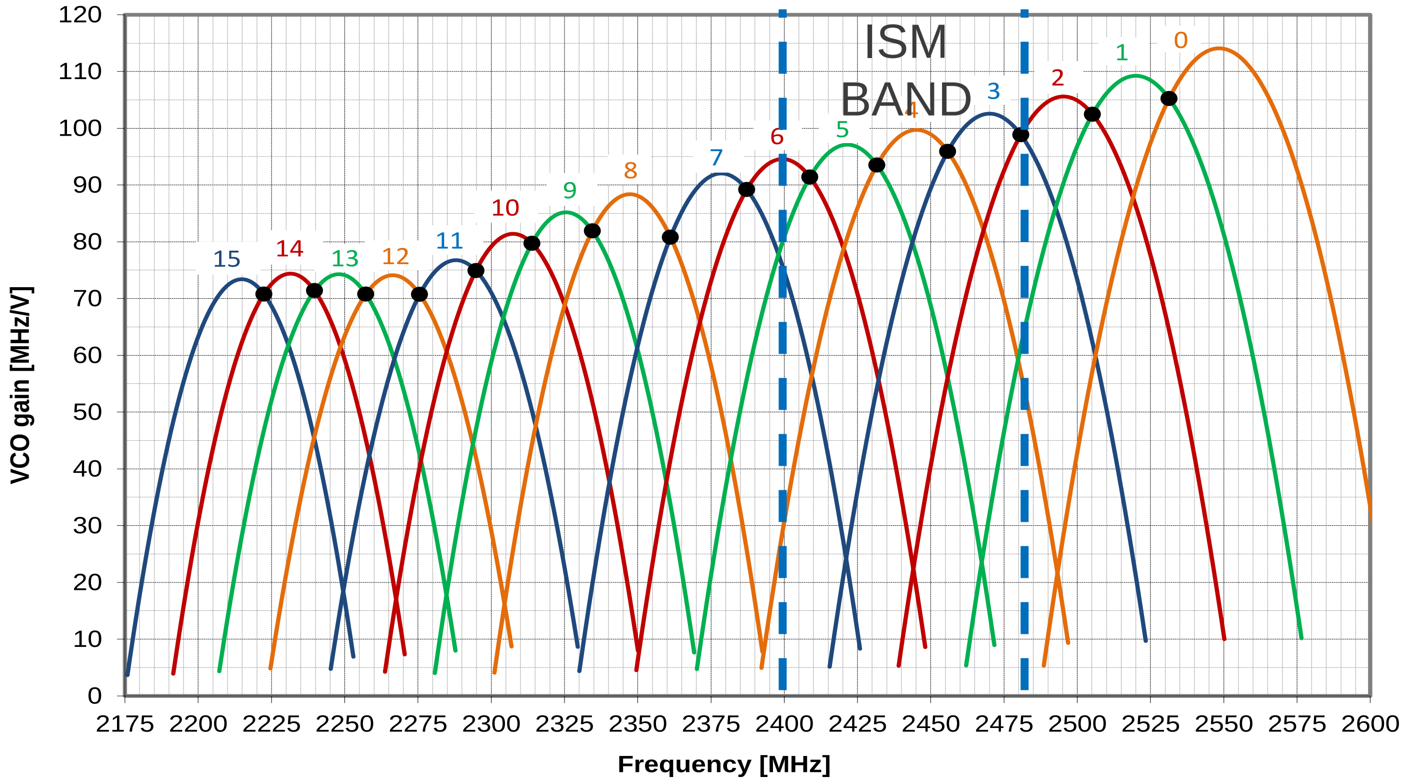
Layout view and things to care about (65nm CMOS)

- Calculate loaded-Q and equivalent series resistor
  - Size routing lines adequately (R vs C trade-off)
- Perform layout extract (RC)
- Investigate where the energy flows
  - Make good virtual ground
  - Optimize Q of each branch
- Evaluate biasing resistors cut-off
  - DC noise up-converted but $R_{RF} << R_{DC}$!
- Connect both gate ends of MOS
  - Calculate R_{GATE} to find max W_G
- Watch-out for vias, evaluate their resistance



VCO is ~50% of PLL area
~0.2x0.3mm^2

Measurements of the VCO gain across its sub-bands

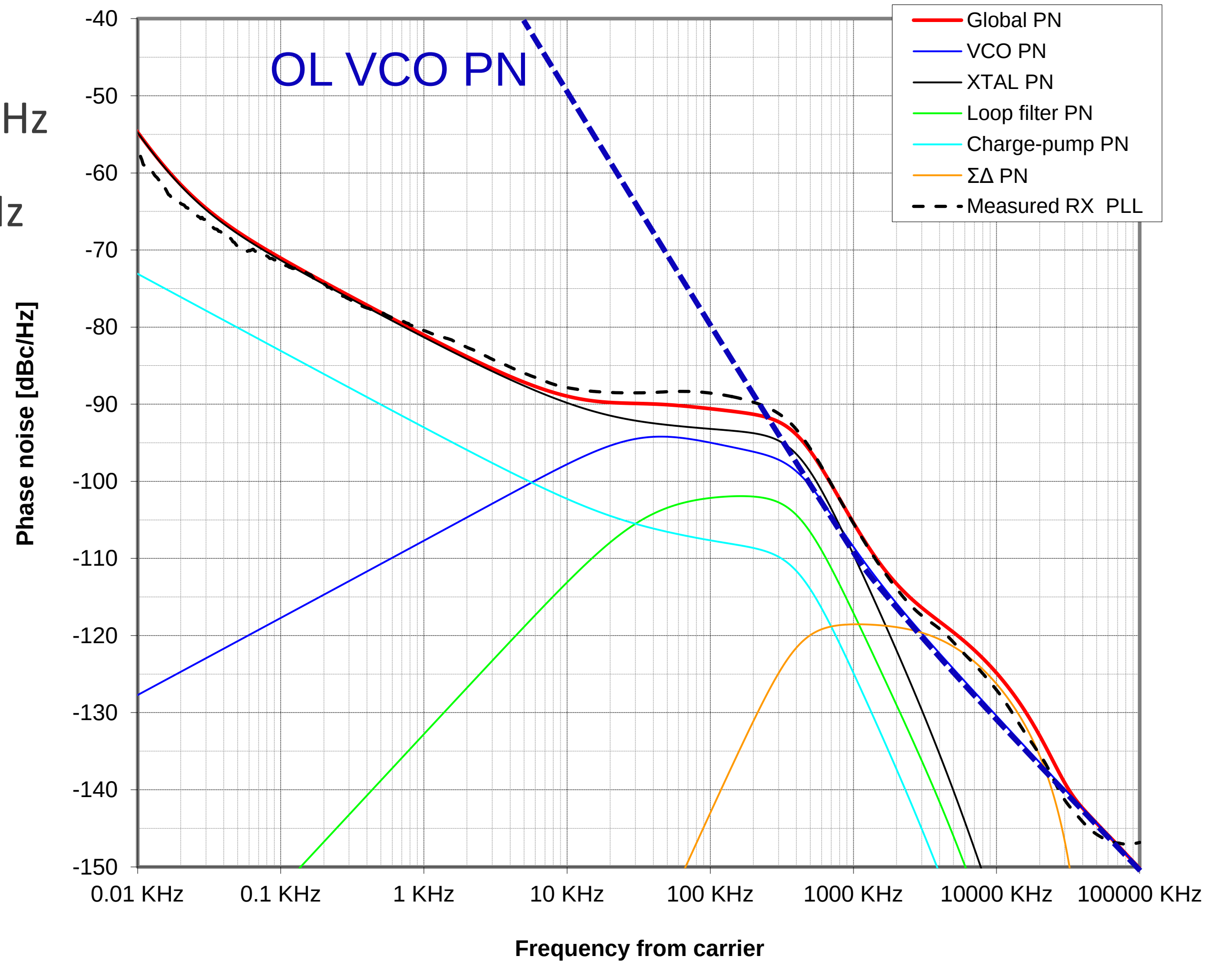


- **Wide frequency range** with 16 sub-bands (±9%)
- Very good overlap
- Almost constant KVCO over 2.4-2.48GHz

2.4GHz PLL phase noise with 48MHz XO and consumption

VCO noise

- 1/f noise corner as high as 1MHz
- PN of -110dBc/Hz @ Δf = 1MHz



Current consumption

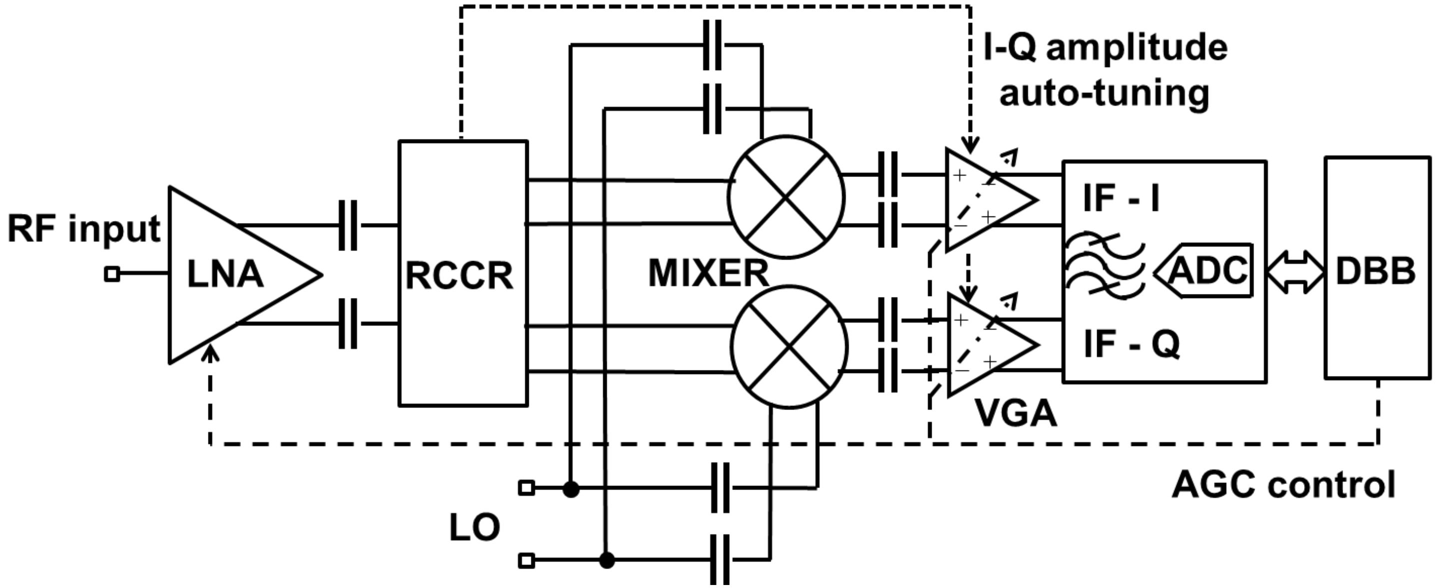
- VCO 850µA
- XO wi buffer 100 µA
- Total PLL 1.5mA

Quadrature generation

- 2 cross-coupled VCOs
- Doubles the power & area, L matching
- LO @ carrier frequency & phase shifter + limiter (RC-CR)
- Power dissipation, Q degradation
- LO @ $2 \cdot f_C$ & ÷2 in quadrature
- Avoids LO pulling, usually better Q, higher power since load is not absorbed by tank
- Phase shifter in RX path
- Linearity, noise figure, LO pulling

Avoiding quadrature generation

- Since quadrature is not required in TX, use RC-CR phase shifter in signal path
- High LNA gain to mitigate 3dB RC-CR loss and NF of passive mixers
  - Compromise on linearity



Quadrature LO generation with source coupled logic divider

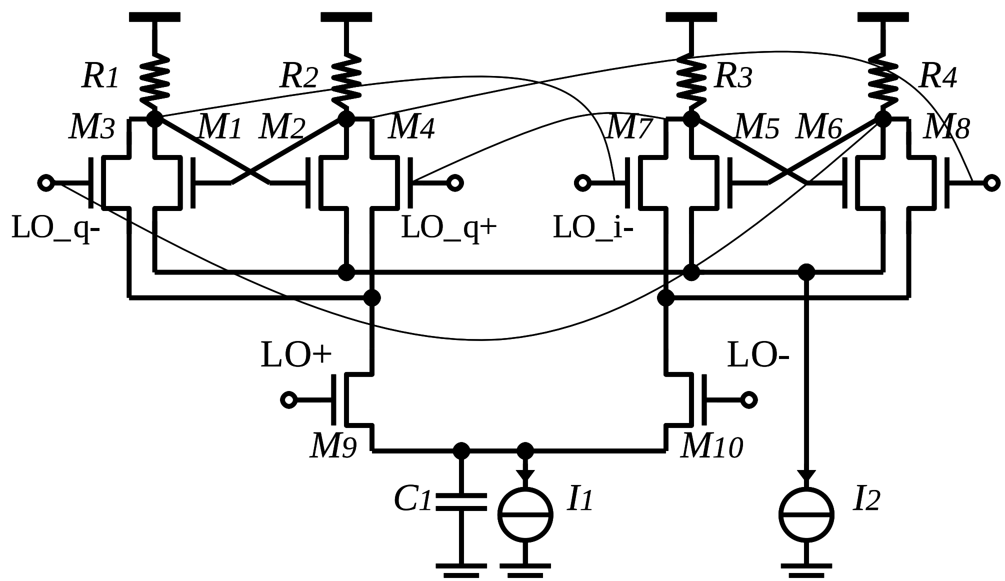
Small signal Kirchhoff equations

$$\begin{bmatrix} 1/R_{1,2} - gm_{1,2} + s\cdot Cp_{1,2} & gm_{7,8} \\ -gm_{3,4} & 1/R_{3,4} - gm_{5,6} + s\cdot Cp_{3,4} \end{bmatrix} \cdot \begin{bmatrix} V_{1,2} \\ V_{3,4} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

Barkhausen criterion

$$\left(1/R_{1,2} - gm_{1,2}\right)\cdot\left(1/R_{3,4} - gm_{5,6}\right) = 0$$

$$s^2 \cdot Cp_{1,2} \cdot Cp_{3,4} - (j)^2 \cdot gm_{3,4} \cdot gm_{7,8} = 0$$



Large signal equations

$$\hat{V} = 2 \cdot \frac{I_{M1}}{gm_{1,crit}} = 2 \cdot R \cdot I_{M1}$$

$$\omega_o = \frac{gm_3}{C} \cdot \frac{I_{M1,crit}}{I_{M1}} \rightarrow \frac{2 \cdot I_{M3}}{C \cdot \hat{V}}$$

if ωo close to $\omega_{LO}/2$, injection locking